Atty. Docket No. PIA31223/DBE/US
Serial No: 10/751,212

Remarks

Applicant and his representatives wish to thank Examiner Ha for the helpful explanations in the Advisory Action dated May 5, 2005. Applicant has addressed the Examiner's concerns regarding the pillar shape of the bump by amending Claim 1 to recite a bump having a pillar shape. The following remarks shall address Examiner's other concerns as indicated in the Office Action dated December 20, 2005.

Claims 1-2 have been amended. Claims 5-18 have been added. Therefore, Claims 1-18 are active in this application. No new matter is introduced by the present Amendment.

The present invention relates to a method for packaging a semiconductor device comprising:

a) forming an Au bump on a bond pad of a wafer,

b) dicing the wafer into a chip, and

c) attaching the Au bump of the chip to a substrate to form a flip-chip bond by using a thermo-pressure process, wherein the Au bump is connected directly to the chip and connected to the substrate through multi-stacked metal layers, and has a pillar shape (see Claim 1 above).

New Claim 10 includes similar limitations.

Although the Office Action appears to assert that the metal balls 80 of Soga et al. (U.S. Pat. Appl. Publ. No. 2002/0171157) correspond to the pillar-shaped Au bump of the present claims, the art also appears to recognize differences between the metal balls 80 of Soga et al. and the pillar-shaped Au bump of the present claims. The present invention thereby enables miniaturization of the semiconductor device, simplification of the packaging process, and reduced costs, relative to the method of Soga et al.

The references cited by the Examiner (Soga et al. and Fukao et al. [U.S. Pat. Appl. Publ. No. 2003/0011078]) neither disclose nor suggest attaching an Au bump on a bond pad of a wafer to a substrate through a plurality of (e.g., multi-stacked) metal layers, wherein the Au bump is

connected directly to the chip and has a pillar shape, as recited in Claim 1. Similarly, the cited references neither disclose nor suggest attaching a pillar-shaped Au bump formed directly on a bond pad of a chip to a substrate through a plurality of metal layers, as recited in Claim 10. Thus, the present claims are patentable over the cited references.

The Rejection of Claims 1-3 under 35 U.S.C. § 102(a)

The rejection of Claims 1-3 under 35 U.S.C. § 102(a) as being anticipated by Soga et al. is respectfully traversed.

Soga et al. disclose junctions formed between a semiconductor device and a substrate, comprising metal balls (Cu, etc.) and compounds of Sn and the metal balls, and the metal balls are bonded together by the compounds (Abstract). With regard to FIGS. 16(a)-(d), Soga et al. disclose a package of a chip 25 and junction substrate 14, obtained by the temperature-hierarchical bonding of Pb-free solder by use of Cu balls 80 (Soga et al., p. 12, paragraph [0115]). As regards the shape of a bump, Soga et al. disclose a ball bump (FIG. 16(b)), a wire bond bump (FIG. 16(c)) and a Cu-plated bump of a readily deformable structure (FIG. 16(d)) (Soga et al., p. 12, paragraph [0115]).

Although Soga et al. use the term "bump" to describe Cu balls 80, it is believed that this term merely refers to a deformed shape of Cu balls 80. For example, Soga et al. teach that in the case shown in FIG. 16(a), Soga et al. form bonds by feeding Sn onto a thin-film pads 82 on the side of the Si chip 25 by vapor deposition, plating, a paste, or the composite paste including metal balls and solder balls; thermally pressure-bonding thereto metal balls 80 such as balls of Cu, Ag, Au, etc. or Au-plated Al balls, or metallized organic resin balls to thereby form an intermetallic compound 84 with Sn; then bonding to a junction substrate (Soga et al., p. 12, paragraph [0115]). This disclosure is consistent with the understanding in the art that solder balls or metal balls are typically used in flip chip bonding (see, e.g., Wolf, Silicon Processing for the VLSI Era, Volume 1 – Process Technology [2nd ed. 2000], p. 858, last 5 lines; previously submitted with the Amendment filed October 12, 2005), whereas Au bumps (as that term is

generally understood in the art) appear to be associated with tape automated bonding (or TAB; see Wolf, p. 854, ll. 2-5 from the bottom, and p. 855, previously submitted with the Request for Reconsideration filed April 20, 2006). Consistent with the understanding in the art, the Au bumps of the present Claims 1 and 10 have a pillar shape (see, e.g., Au bump 200 in FIG. 3A of the present application). Thus, the alternative Au, etc. or Au-plated Al balls that may form the ball bump or wire bond bump of Soga et al. (FIGS. 16(b)-(c)) are different from, and not equivalent to, the pillar-shaped Au bumps recited in Claims 1 and 10 (further compare, e.g., the paragraph bridging pp. 1-2 of the present specification with p. 2, ll. 9-21 of the present specification).

Further, since the metal balls 80 of Soga et al. are ball-shaped, rather than pillar-shaped, the metal balls 80 may have a relatively small contact surface with the chip 25, and it is believed that they cannot be readily attached to the chip 25 and that they may show low interconnectivity. Therefore, it is believed that the metal balls 80 of Soga et al. cannot be directly connected to the chip 25, and that they require the processes of forming thin film pad 82 **and** intermetallic compound 84 to connect the metal balls 80 to the chip 25. In contrast, the Au bumps of the present Claims 1 and 10 have a pillar shape, as stated above. As a result, the presently claimed pillar-shaped Au bumps can be directly connected to the chip (e.g., through an interface metallurgy on a bond pad, as disclosed by Wolf in Fig. 17-11, p. 856, previously submitted with the Request for Reconsideration filed April 20, 2006), without using both the intermetallic compound 84 **and** the thin film pad 82 as disclosed by Soga et al.

Soga et al. also discloses a flip chip mounting structure in FIG. 5(a), in which Si chips 8 are bonded by die bonding while the terminals are connected by wire bonding (see, e.g., Soga et al., page 8, paragraph [0086]). Although Soga et al. discloses Au or Cu bumps 18 of each of the Si chips bonded to the junction substrate 35 by supplying a paste thereto (see, e.g., Soga et al., page 8, paragraph [0086]), the Au or Cu bumps 18 of FIG. 5(a) appear to be metal balls, as disclosed in the Abstract, shown in FIG. 16(a), and as described later in paragraph [0086] (i.e., "where Au ***ball*** bumps are used while Sn-plated terminals are provided on the substrate"; see Soga et al., page 8, paragraph [0086], ll. 26-30; emphasis added).

As was stated earlier, a typical flip chip bonding process does not include the steps of forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate using a thermo-pressure process. A typical flip chip bonding process includes the steps of forming balls on the bond pads, flipping the chip over to place the balls in contact with the substrate, and applying a reflow process to attach the solder balls to the substrate (see, e.g., Wolf, pp. 857-858, previously submitted.) The disclosure of Soga et al. appears to be consistent with this understanding and with Applicant's positions. Therefore, Soga et al. do not disclose or suggest forming an Au bump having a pillar shape on a bond pad and attaching the Au bump connected directly to the chip to a substrate through multi-stacked metal layers, as recited in Claim 1. Similarly, Soga et al. do not disclose or suggest forming a pillar-shaped Au bump directly on a bond pad of a wafer and attaching the pillar-shaped Au bump to a substrate through a plurality of metal layers, as recited in Claim 10.

Consequently, this ground of rejection is unsustainable, and Applicant respectfully requests withdrawal thereof.

The Rejection of Claim 4 under 35 U.S.C. § 103(a)

The rejection of Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Soga et al. and Fukao et al. is respectfully traversed.

As discussed above, Soga et al. is deficient with regard to forming an Au bump having a pillar shape on a bond pad and attaching the Au bump connected directly to the chip to a substrate through multi-stacked metal layers, as recited in the present Claim 1. Fukao et al. fails to cure this deficiency.

The disclosure of Fukao et al. relates to a semiconductor module and producing method therefor (Title). Fukao et al. disclose that a gold bump or a nickel bump 7 is applied to the pad portion 2a of a bare IC chip 2 (see Fukao et al., p. 4, paragraph [0079]). However, Fukao et al. directly connect an end of a lead terminal 3 to the pad portion 2a of the bare IC chip 2 via a bump 7 made of gold, nickel, solder or the like (see Fukao et al., p. 4, paragraph [0080], and

FIG. 2). Therefore, it is believed that Fukao et al. do not disclose or suggest attaching the Au bump of the chip to a substrate to form a flip-chip bond.

As a result, neither Soga et al. nor Fukao et al. appear to disclose attaching an Au bump having a pillar shape on a bond pad of a chip to a substrate through a plurality of (e.g., multi-stacked) metal layers to form a flip chip bond. Therefore, it appears that no combination of the two references can disclose or suggest all of the limitations of Claims 1 or 10, and Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) of Claim 4 (which depends from Claim 1).

Conclusions

In view of the above remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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